

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-1784	SERIAL NO.
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Luan Tran et al.	
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U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,045,899	09/03/91	Arimoto			
	AB	5,107,459	04/21/92	Chu et al.			
	AC	5,350,706	09/27/94	McElroy et al.			
	AD	5,469,383	11/21/95	McElroy et al.			
	AE	5,537,347	07/16/96	Shiratake et al.			
	AF	5,508,541	04/16/96	Hieda et al.			
	AG	5,383,151	01/17/95	Onishi et al.			
	AH	5,726,092	03/10/98	Mathews et al.			
	AI	5,595,928	01/21/97	Lu et al.			
	AJ	5,747,844	05/05/98	Aoki et al.			
	AK	5,665,623	09/09/97	Liang et al.			

FOREIGN PATENT DOCUMENTS							
	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	AL	JP 03205868	09/09/91	Japan			Abs.
	AM						
	AN						
	AO						
	AP						

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)		
	AR	A. Chatterjee et al., "A Shallow Trench Isolation Study for 0.25/0.18 μ m CMOS Technologies and Beyond", IEEE, 1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 156-57 (1996).
	AS	M. Aoki et al., "Fully Self-Aligned 6F ² Cell Technology for Low Cost 1Gb DRAM", IEEE 1996 Symposium on VLSI Technology Digest of Technical Papers, pp. 22-23 (1996).
	AT	J.S. KIM et al., "A Triple Level Metallization Technique for Gigabit Scaled DRAMS", VMIC CONFERENCE, Technology Development, Memory Device Business, Samsung Electronic Co., pp. 28-33 (June 18-20, 1996).

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Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-1784	SERIAL NO.		
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U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,637,528	06/10/97	Higashitani et al.			
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	AR		B. KEETH, "A Novel Architecture for Advanced High Density Dynamic Random Access Memories",				
			A Thesis for M.S. E.E., University of Idaho pp. 1-62 (i-vi); (May 1996).				
	AS		T. Hamamoto et al., "NAND-Structured Trench Capacitor Cell Technologies for 256 Mb DRAM and Beyond",				
			IEICE Transactions On Electronics, pp. 789-796, 1995.				
	AT		M. Noguchi et al., "0.29- μm^2 Trench Cell Technologies for 1G-bit DRAMs with Open/Folded-Bit-Line Layout and Selective Growth Technique",				
			1995 Symposium on VLSI Technology Digest of Technical Papers, pp. 137-138.				
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	AQ						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR		V. Mathews et al., <i>Dry O₂ High Pressure Field Oxidation for 0.25 μm Isolation Technology</i> .				
			SSDM '95 - Device and Process Technology, 2 pages.				
	AS						
	AT						
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